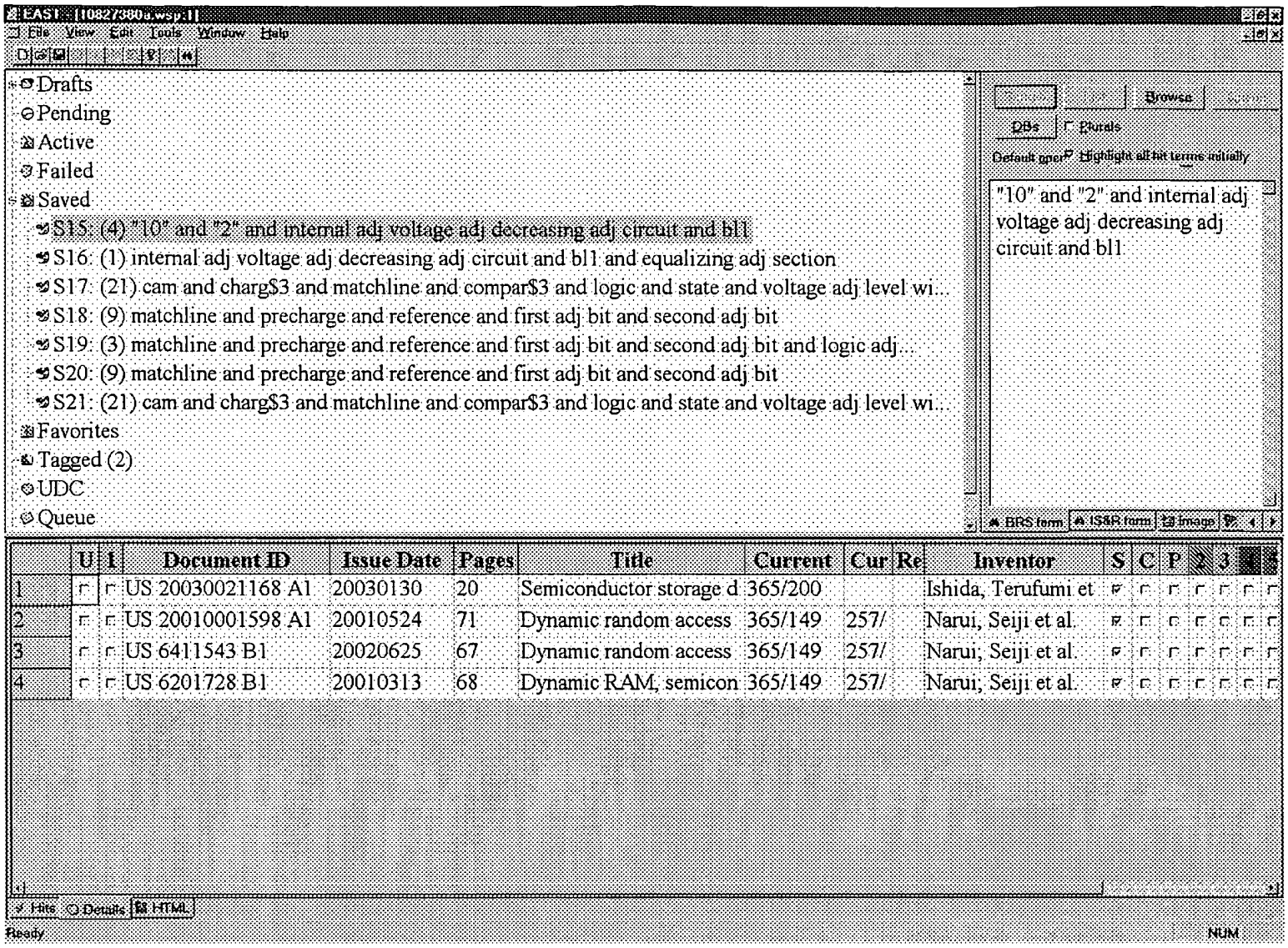
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S15: (4) "10" and "2" and internal adj voltage adj decreasing adj circuit and bl1
S16: (1) internal adj voltage adj decreasing adj circuit and bl1 and equalizing adj section
S17: (21) cam and charg$3 and matchline and compar$3 and logic and state and voltage adj level wi...
S18: (9) matchline and precharge and reference and first adj bit and second adj bit
S19: (3) matchline and precharge and reference and first adj bit and second adj bit and logic adj...
S20: (9) matchline and precharge and reference and first adj bit and second adj bit
S21: (21) cam and charg$3 and matchline and compar$3 and logic and state and voltage adj level wi...
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1 US 20030021168 A1 20030130 20 Semiconductor storage d 365/200 Ishida, Terufumi et
2 US 20010001598 A1 20010524 71 Dynamic random access 365/149 257/ Narui, Seiji et al.
3 US 6411543 B1 20020625 67 Dynamic random access 365/149 257/ Narui, Seiji et al.
4 US 6201728 B1 20010313 68 Dynamic RAM, semicon 365/149 257/ Narui, Seiji et al.
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